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## (54) Integrated circuit with active devices under bond pads.

(57) Active circuitry is placed under the bond pads (3) in an integrated circuit having at least three metal levels (211, 215, 219). The metal level (215) adjacent the bond pad level acts as a buffer and provides stress relief and prevents crack propagation in the dielectric (213) that would otherwise lead to unacceptably large leakage currents.

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## Technical Field

This invention relates generally to the field of integrated circuits and particularly to such integrated circuits in which at least a portion of the active circuitry is positioned under the bond pads.

## Background of the Invention

Although much public attention is given to aspects of integrated circuit technology, such as the number or dimensions of devices in the circuit and their operating speeds, because progress in these aspects has great public appeal, other aspects of integrated circuit technology are of equal importance to progress within the field of integrated circuits. For example, integrated circuits must be electrically contacted. The electrical circuit from the external pins of the integrated circuit package to the integrated circuit goes through bond pads which are located on the periphery of the integrated circuit. The bond pads are metal areas which are electrically connected to the devices in integrated circuit by buffers and electrically conducting interconnects. Due to conventional bonding technology used to, for example, attach wires to the bond pads and to design constraints, the bond pads have relatively large dimensions as compared to the device dimensions and occupy or cover a significant portion of the chip surface. The area underneath the bond pads thus occupies a substantial fraction of the entire chip surface.

The electrical connection between the package and the bond pad requires physical integrity as well as high electrical conductivity. The conventional bonding process used to form the connection typically requires either or both elevated temperatures or high pressures to produce a good connection between the wire and the bond pad. If the bond pad is on a dielectric, the bonding conditions produce thermal and mechanical stresses in the dielectric. The stress may cause defects which result in large leakage currents through the dielectric between the bond pads and the underlying substrate, which is frequently electrically conducting. The leakage currents preclude use of the substrate area under the bond pads for device purposes thereby decreasing the efficiency of substrate utilization for device purposes. The buffers are typically located on the periphery of the integrated circuit and between bond pads to avoid placement under the bond pads; the spacing between bond pads must be increased to accommodate the buffers or other devices.

Attempts have been made to use the substrate under the bond pads for active device purposes. Attempts have been made using conventional wire bonding technology. For example, Mukai et al in IEDM, pp. 62-65, 1981, reported the use of an interlevel dielectric layer between the bond pads and active circuitry to absorb stresses produced by the bonding process. Several dielectric materials were reported. Additionally, Haruta et al reported in Japanese patent JP 58197735 the use of a metal layer to absorb the stresses produced during bonding. It is stated that magnesium is added to the aluminum to strengthen the aluminum and prevent stresses from passing through to the dielectric, and that no cracks were generated in the dielectric. However, if there are defects in the dielectric, current may flow through the dielectric to the active devices.

## Summary of the Invention

According to an exemplary embodiment of this invention, an integrated circuit is fabricated with active circuitry underneath the bond pads. There is a plurality of patterned metal layers between the bond pads and the semiconductor layer with the active devices. There are dielectric layers between the patterned metal layers and the metal layers and the bond pads and the active circuitry. The metal layer nearest the bond pads shields and protects the devices from the stress produced during the bonding process. This metal layer is patterned to form metal regions that are substantially over the active devices and which may be electrically isolated from the integrated circuit. The active devices may be, for example, input/output buffers. The electrical connections between the bond pads and the active circuitry are made through windows in the dielectric layers, between the bond pads and the active devices, which expose portions of the active circuitry and are filled with metal. In a preferred embodiment, the integrated circuit has three metal levels.

## Brief Description of the Drawing

FIG. 1 is a top view of a portion of an integrated circuit according to this invention; and

FIG. 2 is a sectional view of a portion of the integrated circuit according to this invention depicted in FIG. 1.

For reasons of clarity, the elements depicted are not drawn to scale.

## Detailed Description

A top view of a portion of an integrated circuit according to this invention is depicted in FIG. 1. Depicted is integrated circuit chip 1, a plurality of metal bond pads 3, and a dielectric layer which is over the entire chip 1, but has been patterned to expose portions 5 of the metal bond pads 3. The bond pads 3 are formed on the integrated circuit. The primary portion 7 of the integrated circuit is formed in the center of the chip, but the integrated circuit has active devices, for example, input/output buffers, underneath the bond pads

3. There are dielectric layers between the bond pads and a metal layer; and between the metal layers and the active devices. At least one of the metal layers has been patterned to cover the region 9 underneath the bond pads 3 and over active device areas (not shown). The other layers, both metal and dielectric, are not shown for reasons of clarity. The metal layer nearest the bond pad provides the stress relief needed so that the integrity of the intervening dielectric layers is not destroyed during the bonding process. Even if the dielectric between the bond pad and the metal layer nearest the bond pad develops defects during the bonding process, the leakage current stops at the metal layer. The area underneath the bond pads may thus be used for active devices without fear of excessive leakage currents through the dielectric layers. The ability to position active devices underneath the bond pads permits the bond pads to be more closely spaced to each other and thereby allows more bond pads per linear peripheral distance.

The structure of the integrated circuit is better understood by reference to FIG. 2 which is a sectional view of an integrated circuit according to this Invention. A portion of the periphery including the bond pad, metal and dielectric layers and active devices under the bond pad is illustrated. Depicted are substrate 201, devices 203, first dielectric layer 205, second dielectric layer 207, first metal layer 211, third dielectric layer 213, second metal layer 215, fourth dielectric layer 217, third metal layer 219, and fifth dielectric layer 221. There is dielectric material 214 between layers 213 and 217. Wire 223 has been bonded to third metal layer 219 which forms bond pad 9. Second metal layer 215 has been patterned so that a portion underlies the bond pads and covers at least portions of the devices 203. Windows 251 and 255 in dielectric layers 205 and 207 and 217, respectively, provide electrical connections between substrate 1 and metal layer 211, and metal layers 215 and 219, respectively. Second metal layer 215 provides the stress relief during the bonding process that prevents the dielectric layers from cracking. If dielectric layer 217 develops defects during bonding, leakage currents do not flow to the substrate because of the pressure of the metal layer.

Certain features described generally in the preceding paragraph merit more comment and detail. The device 203 depicted is a field effect transistor having a gate structure 231, source/drain regions 233 and 235 on opposite sides of gate structure 231, and insulating sidewalls 237 and 239 on opposite sides of the gate structure 231. Gate structure 231 is formed from polysilicon. Insulating portions of the gate structure, such as the gate oxide, are well known and used not be depicted. First and second dielectric layers 207 and 209 are conformal dielectrics such as TEOS and BPTEOS, respectively. Other dielectric layers can also be formed from well known deposited oxides or nitrides. The metal layers may be aluminum. Additives, such as silicon, may be present in minor amounts. As shown, a portion of the integrated circuit, including active devices such as field effect transistor 203, is formed directly under the bond pad.

The structure depicted will be readily fabricated by those skilled in the art using known techniques. Well known techniques may be used to deposit and pattern the dielectric and metal layers and to form the device. For example, well known lithographic, ion implantation, etching, etc., processes may be used. Detailed description of suitable processes is therefore not required. The details of the integrated circuit will depend upon the applications desired for the integrated circuit. The integrated circuit will be relatively complex, at least by the standards used at the present time, to warrant the use of multilevel metal interconnects. The packaging connection to the bonding pad is done by any of the conventional and well known techniques presently used.

Metal layer 215 may be patterned so that it is smaller than depicted and a window goes directly from the bond pad to the active devices. Layer 215 is then electrically isolated (except for stray capacitance) from the remainder of the integrated circuit. The window is filled with metal using now conventional techniques. This embodiment is desirable because it permits the dielectric layers to be thicker than in the previously described embodiment. Thicker dielectric layers are less likely to crack than are thinner layers.

That the area underneath the bond pads could be used for device purposes was determined by measuring capacitor leakage through a dielectric layer under various bonding conditions. The bonding process stresses the dielectric layer between two metal layers; defects in the dielectric may be produced which result in leakage currents between the metal layers. However, we found that in integrated circuits with three or more levels of metal, the second or higher level or metal can provide stress relief from crack propagation in the dielectric caused by the bonding process.

Variations in the embodiment depicted will be readily thought of by those skilled in the art. Although an embodiment with three metal layers has been described, more metal layers may be present. Additionally, the bond pads need not be on the periphery of the integrated circuit. Furthermore, the bond pads need not be electrically connected to the metal layer immediately underneath.

## Claims

1. An integrated circuit comprising:
   a substrate (201);
   active devices (203) formed on the surface of said substrate (201);

a plurality of bond pads (3), said bond pads (3) being substantially over a portion of said active devices (203);

a plurality of patterned metal layers (215) between said bond pads (3) and said substrate (201), at least of said metal layers (215) being substantially over at least one of said active devices (203);

dielectric material (214, 213, 217) separating said patterned metal layers (215) from each other and from said bond pads (3) and from said active devices (203); and

electrical connections (251, 255, 215) from said bond pads (3) to said active devices (203).

2. An integrated circuit as recited in claim 1 in which said at least one of said patterned metal layers (215) is electrically connected to at least one of said bond pads (3).

3. An integrated circuit as recited in claim 2 in which said at least one of said patterned metal layers (215) is electrically connected to at least one device (203) of said active circuitry under at least one of said bond pads (3).

4. An integrated circuit as recited in claim 1 in which said integrated circuit has three metal levels (211, 215, 219).

5. An integrated circuit as recited in claim 1 in which said integrated circuit has at least four metal levels (211, 215, 219).

6. An integrated circuit comprising:

a substrate (201);

active devices (203) formed on the surface of said substrate (201);

a plurality of bond pads (3), at least one of said bond pads (3) being substantially over at least one of said active devices (203);

a patterned metal layer (215) between said plurality of bond pads (3) and said substrate (201), at least a portion of said metal layers (215) being substantially over at least one of said active devices (201);

dielectric material (213, 214, 217) separating said patterned metal layer (215) from said bond pads (3) and from said active devices (203); and

electrical connections (251, 255, 215) from said bond pads (3) to said active devices (203).

7. An integrated circuit as recited in claim 6 further comprising a metal layer (211) between said patterned metal layer (215) and said active devices (203); said metal layer (211) being separated from said active devices (203) and said patterned metal layer (215) by dielectric material (213).

*FIG. 1*

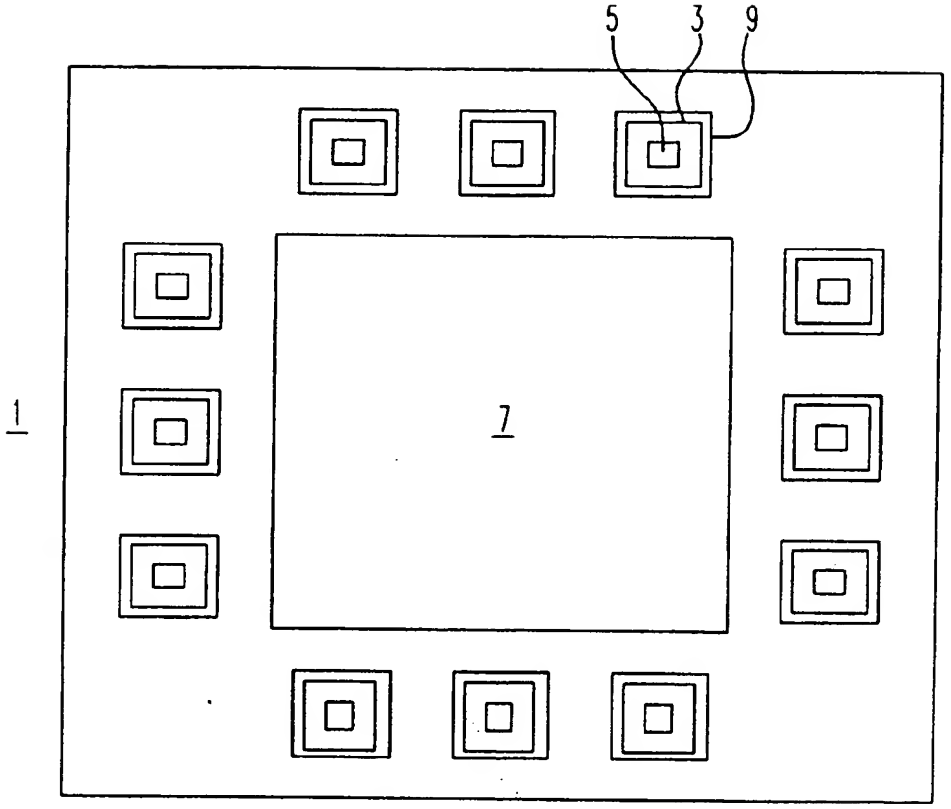
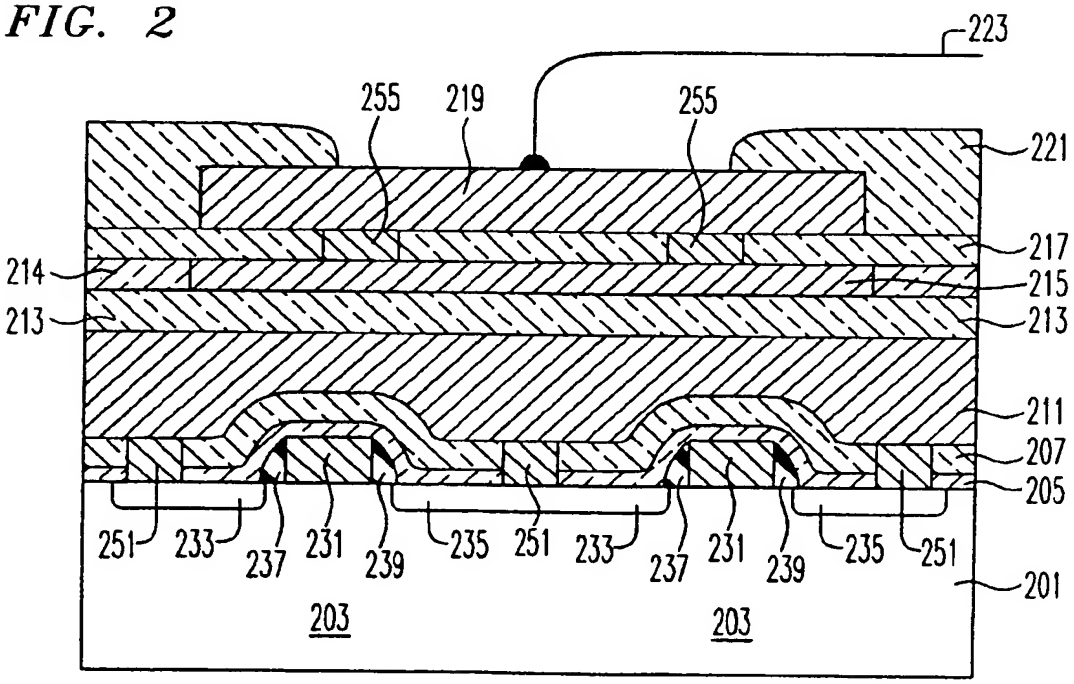



*FIG. 2*



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# EUROPEAN SEARCH REPORT

Application Number
EP 94 30 5566

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int.Cl.6) |
|---|---|---|---|
| A | EP-A-0 100 100 (KABUSHIKI KAISHA TOSHIBA) 8 February 1984<br>* page 6, line 6 - page 7, line 7; claims 1-4; figures 2-5 * | 1,3,6 | H01L23/485 |
| A | EP-A-0 418 777 (FUJITSU LTD.) 27 March 1991<br>* claims 1,3,6; figure 6K * | 1 | |
| A | PATENT ABSTRACTS OF JAPAN<br>vol. 10, no. 228 (E-426) (2284) 8 August 1986<br>& JP-A-61 064 147 (NEC CORP) 2 April 1986<br>* abstract * | 1,2 | |

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H01L

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 28 November 1994 | Fransen, L |

CATEGORY OF CITED DOCUMENTS

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